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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/764,880	01/23/2001	Takeo Matsuki	OSP-10057	4114

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EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/764,880	MATSUKI ET AL.	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004, 8/1/2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. In response to Applicant communication on 3/2/2004 the restriction requirement by the Office action issued on 9/13/2002 is withdrawn.

2. Claims 1-17 are pending in the Application.

3. This is in response to Applicant's Amendment filed on August 1st 2002.

Note that the figures and reference numbers referred to in this Office Action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 4, 5, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakoh (US. Patent 5641991).

REGARDING TO CLAIM 1

Sakoh discloses the invention of the structure for a semiconductor device (fig 6 and

Claim 1 column 9 lines 50-67), provided with a contact plug, which is formed by forming a contact hole through a first interlayer insulating film on a silicon substrate (fig 6 reference numeral 1) and by filling the contact hole (fig 6 reference numeral 9 with silicon, comprising: a silicide pad (fig 5 reference numeral 12) formed on the top surface of the silicon plug in a self-aligning manner and having a diameter which is larger than that of the silicon plug; wherein, the top surface of the silicide pad is formed above the top surface of the first interlayer insulating film.

REGARDING TO CLAIM 2

Sakoh in his invention (fig 2F and column 4 line 19-22) disclosed a structure of semiconductor device with the silicide pad formed by a refractory metal silicide

REGARDING TO CLAIM 4

Sakoh in his invention discloses (fig 2 to fig 7) a method for manufacturing a semiconductor device, provided with a contact plug, which is formed by opening a contact hole through a first interlayer insulating film (fig 3 layer 3) formed on a silicon substrate (fig 3 layer 1) and filling the contact hole with silicon, comprising the steps of: forming a first insulating film on the silicon substrate; forming a contact hole (fig 3C layer 9) through the first interlayer insulating film; filling the contact hole with a silicon plug; and forming a silicide pad having a larger diameter than that of the silicon plug in a self-aligning manner; wherein, the top surface of the silicide pad is disposed above the top surface of the first interlayer insulating surface (fig 3F).

REGARDING TO CLAIM 5

Sakoh disclose a method for manufacturing a semiconductor device with the step of forming silicide pads that includes the steps of: selectively and partially removing the insulating film and silicon at least in the vicinity of contact plug (fig 4E and 4F) such that the plug protrudes; depositing a refractory metal film (fig 4F layer 12); converting the refractory metal film into the refractory metal silicide by a heat treatment (column 6 lines 23-25); and removing refractor metal film remaining without being converted into silicide and reaction products between refractory metal and an atmospheric gas during the heat treatment.

REGARDING TO CLAIM 7 AND 8

Sakoh discloses a structure of a semiconductor device, (fig 6 and 7) comprising: a silicon substrate, a first interlayer insulating film having a first surface connected to substrate, a polysilicon contact plug formed through the first interlayer insulating film having a top end surface and a top side surface protruding from a second surface of the first insulating layer; a silicide pad formed covering top end surface and topside surface of polysilicon contact plug in a self-aligning manner, a silicide pad made from a refractory metal silicide having a diameter which is larger than a diameter of the polysilicon contact plug, and the silicide pad being above second surface of first interlayer insulating film.

Claim Rejections - 35 USC § 103

6. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art

are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakoh (US patent 5641991) in view of Iwata et al. (US patent 6291861).

REGARDING TO CLAIM 3

Sakoh discloses all the invention and also shows the use of titanium silicide (column 6 line 24) while Iwata et al. show (column 19 line 29-30) the use of the silicide pad with Cobalt as the refractory metal.

It would have been obvious at the time the invention was made for a person of ordinary skill in the art to form structure for a semiconductor device, provided with a contact plug, which is formed by forming a contact hole through a first interlayer insulating film on a silicon substrate and by filling the contact hole with silicon, comprising: a silicide pad formed on the top surface of the silicon plug in a self-aligning manner and having a diameter which is larger than that of the silicon plug; wherein, the top surface of silicide pad is formed above the top surface of the first interlayer insulating film and the refractory metal silicide is of titanium silicide or cobalt silicide.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivated to form a semiconductor device with reduce resistance and low parasitic capacitance.

REGARDING TO CLAIM 6

Sakoh discloses all the invention and also shows the use of titanium silicide (column 6 line 24) while Iwata et al. show (column 19 line 29-30) the use of the silicide pad with Cobalt as

the refractory metal

It would have been obvious to one of ordinary skill in the art the time the invention was made to use the teachings of Sakoh and Iwata et al in order to formulate a method of Manufacturing for a semiconductor device, provided with a contact plug, which is formed by opening a contact hole through a first interlayer insulating film, formed on a silicon substrate and filling the contact hole with silicon, comprising the steps of: forming a first insulating film on the silicon substrate; forming the contact hole through first interlayer insulating film; filling contact hole with a silicon plug; and forming a silicide pad having a larger diameter than that of silicon plug in a self-aligning manner; wherein, the top surface of silicide pad is disposed above the top surface of first interlayer insulating surface.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivated to form a semiconductor Device with reduce resistance and low parasitic capacitance.

8. Claims 9 and 15 are rejected under 35 U.S.C. 103 (a) under Sakoh (US patent 5641991) in view of Wieczorek et al. (US patent 6271122) and in view of further remark.

REGARDING TO CLAIM 9

Sakoh discloses all the invention except for using molybdenum, tantalum, and cobalt Silicide; however Wieczorek et al. (in column 4 lines 44-50) disclose the use of molybdenum Tantalum and cobalt silicide.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the teachings of Sakoh and Wieczorek et al. in order to form a

metal structure that has titanium, tungsten, molybdenum, tantalum and cobalt silicide.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivated to built a semiconductor Device with reduced contact resistance in local interconnects.

REGARDING TO CLAIM 15

Sakoh discloses all the invention except for using molybdenum, tantalum, cobalt Silicide . however Wieczorek et al. (in column 4 lines 44-50) disclose the use of molybdenum tantalum and cobalt silicide and the doping of polysilicon is considered an routine obvious choice of of design that is old and well known in the art.

A person skilled in the art at the time the time the invention was made would have been able to use the teachings of Sakoh, Wieczorek et al. and his routine design skill in order to come up with the invention of claim 15.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable under Sakoh (US patent 5641991) in view of Wu et al. (US patent 5998251), Wieczorek et al. (US paten 6271122) and in view of further remark. Wu et al. disclose the invention of a semiconductor device that use tungsten conductive plug (column 6 line 64) a second interlayer insulating film (fig 15 layer 170) and the use aluminum copper layer for conductive layer is old and well known in the art.

It would have been obvious at the time the invention was made for a person of ordinary skill in the art to use the teachings of Sakoh and Wu et al. in order to built a tungsten plug on top of the silicide pad with an extra layer of aluminum copper alloy.

The reasoning is as follows: A person of ordinary skill in the art would have been Motivated to built a semiconductor device that can connect different layer and that has low

Contact resistance.

10. Claims 11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable under Sakoh (US patent 5641991) in view of Huang (US patent 6096595).

REGARDING TO CLAIM 11

Sakoh discloses all the invention except for the step of forming a second interlayer film on the silicide pad however Huang shows how to form a second insulating layer (fig 15 layer 27) on top of the first insulating layer

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the teachings of Sakoh and Huang in order to fabricate a structure of a semiconductor device, comprising: a silicon substrate; a first interlayer insulating film having a first surface on the substrate; a polysilicon contact plug through the first interlayer insulating film; a silicide pad formed on a first surface of polysilicon contact plug in a self aligning manner and having a diameter, which is larger than the polysilicon contact plug, a first surface of silicide pad being above a second surface of the interlayer insulating film; and a second interlayer insulating film on the first interlayer insulating film on the silicide pad.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivated to built semiconductor with multi-insulating layers that has reduced contact resistance.

REGARDING TO CLAIM 12

Huang shows how to built an upper plug on the polysilicon plug and through the

second interlayer insulating film and aligned with a center of the polysilicon contact plug;

The rationale for combining the teachings by Huang with the teachings of Sakoh has been discussed in the rejection of claim 11.

11. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakoh (US patent 5641991) in view of further remark.

REGARDING TO CLAIM 13

Sakoh discloses all the invention except for showing the step of doping the polysilicon plug, however this is considered a routine skill in the art.

It would have been obvious at the time the invention was made for a person of ordinary skill in the art to use the teachings of Sakoh and his routine skill in order to formulate a method for manufacturing a semiconductor device, comprising the steps of: forming a silicon substrate; forming a first interlayer insulating film above the silicon substrate; forming a first contact hole though the first interlayer insulating film; forming a polysilicon layer on the first interlayer insulating film, the polysilicon layer filling the contact hole and forming a polysilicon plug; doping the polysilicon plug with an impurity having an impurity concentration of between 1 x 10^{20} and 1.5 x 10^{20} cm-3; and forming a silicide pad in a self-aligning manner on the polysilicon plug, the silicide pad having a diameter larger than the diameter of the polysilicon plug, the first surface of the silicide pad being disposed above an upper surface of the first interlayer insulating film.

The reasoning is as follows:

A person of ordinary skill in the art would have been motivated to doped the polysicon plug with a right amount of dopant concentration in order to formulate a method to make semiconductor device that has reduce contact resistance.

REGARDING TO CLAIM 14

Sakoh in his invention discloses a method for manufacturing a semiconductor device, (fig 2A to fig 6 and column 6 lines 23-25, summary of the invention and detailed description of the invention) wherein the steps of forming the polysilicon layer and the silicide pad include the steps of: selectively and partially removing the first insulating film and the polysilicon layer at least in the vicinity of the polysilicon plug such that the polysilicon plug protrudes from the first interlayer insulating layer; depositing a refractory metal film over the polysilicon plug and the first interlayer insulating layer; heat treating the refractory metal film, heat-treating step converting first sections of the refractory metal film into a refractory metal silicide and forming reaction products; removing the second sections of the refractory metal film that were not converted into refractory metal silicide, the first sections being the silicide pad; and removing the reaction products that were formed during the heat-treating step.

The rationale why claim 14 is obvious over Sakoh has been discussed in the rejection of claim 13.

12. Claim 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable under Sakoh (US patent 5641991) in view of Wu et al. (US patent 5998251), Wieczorek et al. (US Patent 6271122) and in view of further remark; all of these inventions disclose in one way or

Another different method of making multiplayer inter-connections in a self-aligned manner.

REGARDING TO CLAIM 16

Sakoh discloses all the invention except for explicitly teach the formation of a second Insulating layer on top of the first insulating layer and the use of tungsten conductive plug and tungsten connecting layer; however Wu et al teach the formation of and upper insulating layer (fig 15 layer 170) and tungsten conductive layer (layer 182 fig 15) and Wieczorek et al. teach how to fabricate a tungsten conductive plug on top of a silicide liner.

It would have been obvious for a person of ordinary skill in the art at the time the Invention was made to use the teachings of Sakoh, Wu et al., and Wieczorek et al. in order to formulate a method for manufacturing comprising the step of: forming a second interlayer insulating film on the first interlayer insulating film and on the silicide pad; forming a second contact hole through the second interlayer insulating film, the second contact hole extending to the silicide pad; forming a titanium nitrite layer on walls of the second contact hole and on the silicide pad; filling the contact hole with tungsten to form a tungsten plug, the tungsten plug contacting the titanium nitrite layer and being connected to the polysilicon plug through the silicide pad and being aligned with a center of the polysilicon plug; and forming a tungsten layer on the second interlayer insulating film and contacting the tungsten plug.

The reasoning is as follows: a person of ordinary skill in the art would have been Motivated to built a semiconductor with reduced resistance that have less material loss And that have high speed logics.

REGARDING TO CLAIM 17

Sakoh discloses all the invention except for explicitly teach the formation of a second

Insulating layer on top of the first insulating layer and the use of tungsten conductive plug and tungsten connecting layer; however, Wu et al teach the formation of and upper insulating layer (fig 15 layer 170) and tungsten conductive layer (layer 182 fig 15) and Wieczorek et al. teach how to fabricate a tungsten conductive plug on top of a silicide liner.

It would have been obvious for a person of ordinary skill in the art at the time the Invention was made to use the teachings of Sakoh, Wu et al., and Wieczorek et al. in order to formulate a method for manufacturing a semiconductor device, comprising the steps of: forming a silicon substrate; forming a first interlayer insulating film above the silicon substrate; forming a first contact hole though the first interlayer insulating film; forming a polysilicon layer on the first interlayer insulating film, the polysilicon layer filling the contact hole and forming a polysilicon plug; forming a silicide pad in a self-aligning manner on the polysilicon plug, the silicide pad having a diameter larger than a diameter of the polysilicon plug, a first surface of the silicide pad being disposed above an upper surface of the first interlayer insulating film forming a second interlayer insulating film on the first interlayer insulating film and on the silicide pad; forming a second contact hole through the second interlayer insulating film, the second contact hole extending to the silicide pad; forming a titanium nitrite layer on walls of the second contact hole and on the silicide pad; filling the contact hole with tungsten to form a tungsten plug, the tungsten plug contacting the titanium nitrite layer and being connected to the polysilicon plug through the silicide pad and being aligned with a center of the polysilicon plug; and forming a tungsten layer on the second interlayer insulating film and contacting the tungsten plug .

The reasoning is as follows: a person of ordinary skill in the art would have been

Motivated to built a semiconductor with reduced resistance that have less material loss and that have high-speed logics.

13. Applicant's arguments with respect to claims 1-17 filed on August 1st 2002 have been fully considered but they are not persuasive.

Even though Applicant uses about six pages of remarks with arguments to rebut the rejections of different claims there are only two main points that the examiner will address to show that the rebuttal is unpersuasive.

They are the followings:

A/ Applicant claims that **Sakoh only discloses that the silicide pad is self-aligned with polysilicon layer and therefore fails to anticipate claims 1,2,4,5,7, and 8 since these claims Have a limitation that the silicide layer is self aligned with the silicon plug.**

The Examiner respectfully disagree since even Sakoh only mentioned the silicide layer is self aligned with polysilicon layer (4) it can be seen clearly on fig 2F and 4F that **this polysilicon layer 4 (the one that surrounds the plug) is inherently self aligned with the silicon plug.**

Thus, the silicide layer is self-aligned with both the polysilicon layer 4 and the silicon plug 9 and therefore, Sakoh correctly anticipated amended claims 1,2,4,5,7 and 8.

B/Applicant claims that Sakoh fails to teach a conductive plug that protrudes is unpersuasive because Sakoh does teach this feature in lines 10-11 of the abstract and in column 1 lines 26-30.

14. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Nguyen et al. (US patent 5,914,518) disclose a Method of forming a metal contact to landing pad structure in an integrated circuit

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9.00 am to 6.00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Thinh T Nguyen TTN

Art unit 2818

David Nelms
Supervisory Patent Examiner
Technology Center 2800